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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/673,541	09/30/2003	Tetsuya Okada	2905-106	1842

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EXAMINER	
RICHARDS, N DREW	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 04/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

SM

Office Action Summary	Application No.	Applicant(s)	
	10/673,541	OKADA ET AL.	
	Examiner	Art Unit	
	N. Drew Richards	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) *9-13* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 14-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 February 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings were received on 2/17/05. These drawings are acceptable.

Claim Objections

Claim 5 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. In view of the added limitations to parent claim 1, the further limitations recited in claim 5 do not further limit the scope of claim 1. Reciting "each [first reverse-conduction type semiconductor regions] spaced substantially equidistant from one another" in claim 1 is essentially alternative wording for "respective neighboring first reverse-conduction type semiconductor regions are disposed so as to be spaced from one another at substantially equal intervals" as recited in claim 5. Thus claim 5 is not considered to further limit claim 1.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-8 and 14-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Buchanan, Jr. et al. (US Statutory Invention Registration No. H40).

Buchanan, Jr. et al. disclose a semiconductor device in figures 1-8 and on columns 1-6. As an example, Buchanan, Jr. et al. disclose a semiconductor device comprising:

a one-conduction type semiconductor substrate 10 (figure 2);

a one-conduction type semiconductor layer 12 formed on the substrate 10 (figure 2);

a plurality of first reverse-conduction type semiconductor regions 22 (figure 2), each designed to have an orthohexagonal shape formed to be spaced substantially equidistant from one another in the semiconductor layer 12 (figure 3);

a second reverse-conduction type semiconductor region 20 forming a boundary in the semiconductor layer 12 so as to surround the plurality of first reverse-conduction type semiconductor regions 22 (figure 2); and

a metal layer 16 forming Schottky junctions in cooperation with the semiconductor layer 12 and surfaces of the fist reverse-conduction type semiconductor regions 22 (figure 2).

With regard to claim 2, the first reverse-conduction type semiconductor regions 22 are buried reverse-conduction type semiconductor material in trenches having an orthohexagonal shape in the semiconductor layer 12.

With regard to claim 3, the first reverse-conduction type semiconductor regions 22 are diffused regions of reverse-conduction type impurities in the semiconductor layer 12.

With regard to claim 4, the plurality of first reverse-conduction type semiconductor regions 22 are disposed so as to be spaced from one another at such intervals that the semiconductor layer 12 between neighboring first reverse-conduction type semiconductor regions is fully depleted when reverse voltages are applied. See figure 2 and column 4 lines 5-12 which discloses the first reverse-conduction type semiconductor regions 22 being spaced apart such that their depletion regions merge under application of a reverse bias.

With regard to claim 5, respective neighboring first reverse-conduction type semiconductor regions 22 are disposed so as to be spaced apart from one another at substantially equal intervals (figure 3).

With regard to claim 6, the first reverse-conduction type semiconductor regions 22 are formed with a thickness smaller than the thickness of the semiconductor layer 12 (figure 2).

With regard to claim 7, the second reverse-conduction type semiconductor region 20 is a diffusion region.

With regard to claim 8, the second reverse-conduction type semiconductor region 20 comprises buried semiconductor material in a plurality of trenches formed in the semiconductor layer 12.

With regard to claim 14, Buchanan, Jr. et al. disclose a semiconductor device comprising:

a one-conduction type semiconductor substrate 10 (figure 2);

a one-conduction type semiconductor layer 12 formed on the substrate 10 (figure 2);

at least one reverse-conduction type semiconductor regions 20/22 formed in the semiconductor layer 12 (figure 2), each designed to have an orthohexagonal shape (figure 3);

a metal layer 16 forming a Schottky junction area in cooperation with the semiconductor layer 12 and surfaces of the at least one reverse-conduction type semiconductor regions 20/22 (figure 2); and

the at least one reverse-conduction type semiconductor region 20/22 is configured such that the semiconductor layer 12 in a Schottky junction area (the area within the ring created by region 20) is fully depleted when a reverse voltage is applied (figure 2; column 4 lines 8-9).

With regard to claim 15, the at least one reverse-conduction type semiconductor region includes:

a plurality of first reverse-conduction type semiconductor regions 22 formed in the semiconductor layer (figure 2); and

a second reverse-conduction type semiconductor region 20 forming a boundary in the semiconductor layer 12 so as to surround the plurality of first reverse-conduction type semiconductor regions 22 figure 2).

With regard to claim 16, Buchanan, Jr. et al. disclose a semiconductor device comprising:

a substrate 10 (figure 2);

a semiconductor layer 12 formed on the substrate 10 (figure 2);

a metal layer 16 forming a Schottky junction area in cooperation with the semiconductor layer 12 (figure 2); and

means for fully depleting the semiconductor layer 12 of carriers in the Schottky junction area when a reverse voltage is applied such as to pinch off the semiconductor layer so as to suppress an IR leak current, where in the means for fully depleting includes a plurality of first reverse-conduction type semiconductor regions 22 each designed to have an orthohexagonal shape foemdin the semiconductor layer and a second reverse-conduction type semiconductor region 20 forming a boundary in the semiconductor layer so as to surround the plurality of first reverse-conduction type semiconductor regions 22 (figures 2 and 3).

Response to Arguments

4. Applicant's arguments with respect to claims 1-8 and 14-16 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (571) 272-1736. The examiner can normally be reached on Monday-Friday 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NDR

GEORGE ECKERT
PRIMARY EXAMINER